# EXHIBIT A

## PENDING CLAIMS

1. A device comprising:

a substrate having a first conductivity type region , wherein the substrate has inwardly concaved recesses having inflection points;

a gate dielectric formed on the first conductivity region of the substrate between the recesses;

a gate electrode formed on said gate dielectric, said gate electrode having a lower portion formed directly on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and

a first silicon or silicon alloy layer in the inwardly concaved recesses that forms a pair of inwardly concaved source/drain regions of a second conductivity type having extensions at the inflection points on opposite sides of said gate electrode, wherein the pair of inwardly concaved source/drain regions have an abrupt junction between the first conductivity type region and the first silicon or silicon alloy layer filling the inwardly concaved recesses at the inflection points, wherein the pair of the inwardly concaved source/drain regions have extensions at the inflection points determined by the inwardly concaved recesses creating metallurgical inflection points directly beneath said lower portion of said gate electrode formed directly on said gate dielectric layer, and directly define a first channel region having a first metallurgical channel length directly beneath said lower portion of said gate electrode in said first conductivity type region, and a second channel region having a second metallurgical length between said metallurgical

inflection points, wherein said first metallurgical channel length directly beneath said lower portion of said gate electrode is larger than said second metallurgical channel length between said metallurgical inflection points.

2. The device of claim 1 wherein said silicon or silicon alloy source/drain regions extend above said gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric.

3. The device of claim 1 wherein said gate dielectric layer is thicker beneath outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode.

4. The device of claim 2 wherein said gate dielectric layer is thicker beneath said sidewall spacer and said outside edge of said gate electrode then the gate dielectric layer beneath the center of said gate electrode.

5. The device of claim 1 further comprising a second silicon or silicon alloy layer having a first conductivity type formed in the recesses between said first silicon or silicon alloy layer and said first conductivity type region.

6. The device of claim 5 wherein said second silicon or silicon alloy layer has a concentration that is greater than the concentration of said first conductivity type region.

7. (Canceled).

8. The device of claim 1 wherein said first conductivity type is n-type conductivity and wherein said second conductivity type is p-type conductivity.

9. The device of claim 1 wherein said first conductivity type is p-type conductivity and wherein said second conductivity type is n-type conductivity.

10. (Canceled).

11. The device of claim 1 wherein said first silicon or silicon alloy layer has a concentration of impurities in a range between $1\text{x}10^{18}/\text{cm}^3$ to $3\text{x}10^{21}/\text{cm}^3$.

12. The device of claim 1 further comprising silicide formed on said silicon or silicon alloy source/drain regions.

13. A device comprising:

a substrate that has a first conductivity type region and inwardly concaved recesses having inflection points;

a gate dielectric formed on the first conductivity type region of the substrate between the recesses;

a gate electrode formed on said gate dielectric, said gate electrode having a lower portion formed directly on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and

a silicon-germanium alloy layer having a second conductivity type in the inwardly concaved recesses that forms a pair of inwardly concaved source/drain regions on opposite sides of said gate electrode with extensions directly beneath said lower portion of said gate electrode having an abrupt junction between the silicon germanium alloy filling the inwardly concaved recesses at the inflection points and the first conductivity type region, wherein said silicon germanium alloy layer extends above the height of said gate dielectric layer wherein the top surface of said silicon-germanium alloy is spaced further from said gate electrode than said silicon-germanium alloy adjacent to said gate dielectric.

14. The device of claim 13 wherein said gate dielectric layer is thicker beneath said outside edges of said gate electrode then the gate dielectric beneath the center of the gate electrode.

15. A device comprising:

a substrate that has a first conductivity type region and inwardly concaved recesses, having inflection points;

a gate dielectric formed on the first conductivity type region of the substrate between the recesses;

a gate electrode formed on said gate dielectric, said gate electrode having a lower portion formed directly on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and

a silicon-germanium alloy layer having a second conductivity type in the inwardly concaved recesses that forms a pair of inwardly concaved source/drain regions of a second conductivity type having a concentration of impurities in a range of $1x10^{18}/cm^3$ – $3x10^{21}/cm^3$ at opposite sides of said gate electrode with extensions directly beneath said lower portion of said gate electrode having an abrupt junction between the first conductivity type region and the silicon-germanium layer filling the inwardly concaved recesses at the inflection points, wherein the pair of the inwardly concaved source/drain regions have the extensions at the inflection points determined by the inwardly concaved recesses creating metallurgical inflection points directly beneath said lower portion of said gate electrode formed directly on said gate dielectric layer to define a first channel region having a first metallurgical channel length directly beneath said lower portion of said gate electrode in said first conductivity type region, and a second channel region having a second metallurgical length between said metallurgical inflection points, wherein said first metallurgical channel length directly beneath said lower portion of said gate electrode is larger than said second metallurgical channel length between said metallurgical inflection points.

# EXHIBIT B

Figure 1

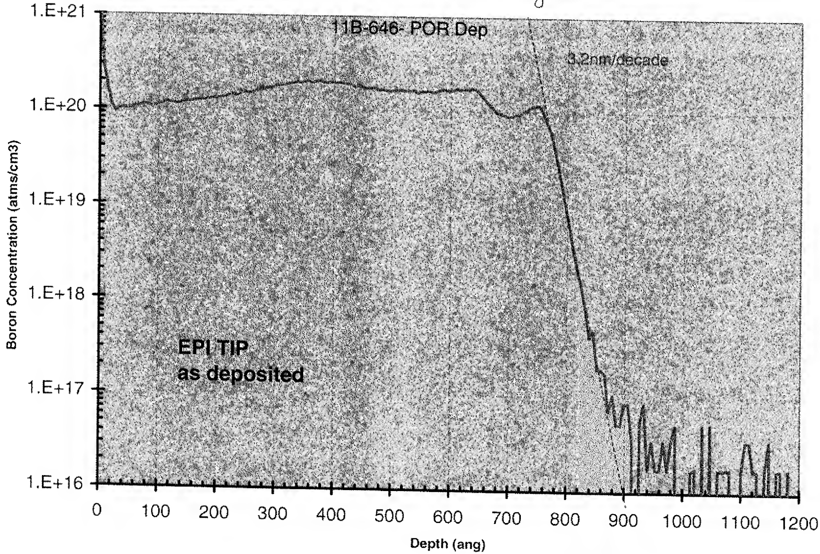
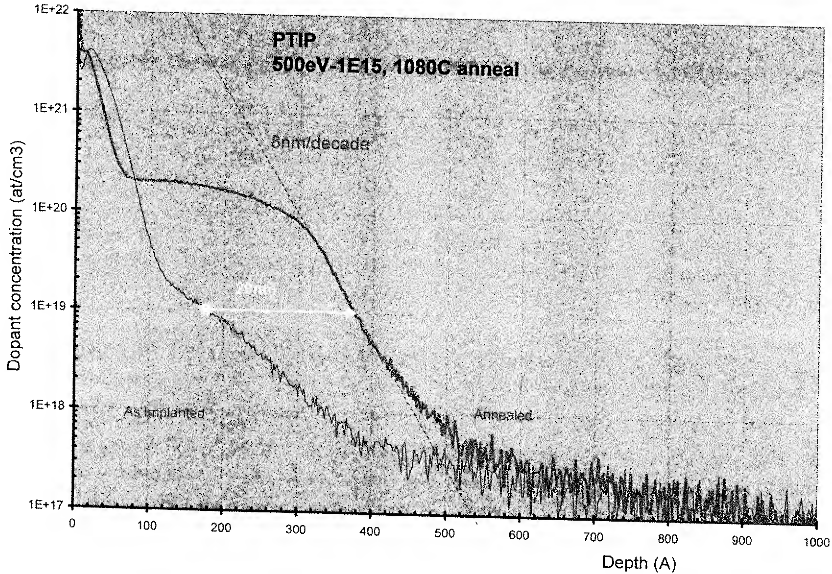

11B-646- POR Dep
3.2nm/decade
EPI TIP
as deposited
Boron Concentration (atms/cm3)
1.E+21
1.E+20
1.E+19
1.E+18
1.E+17
1.E+16
0
100
200
300
400
500
600
700
800
900
1000
1100
1200
Depth (ang)

Figure 2


PTIP
500eV-1E15, 1080C anneal
6nm/decade
As implanted
Annealed
Dopant concentration (at/cm3)
Depth (A)
1E+22
1E+21
1E+20
1E+19
1E+18
1E+17
0
100
200
300
400
500
600
700
800
900
1000